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DESIGN OF A DIGITAL PHASE-LOCKED-LOOP CMOS UNIVERSAL ARRAY.(U)
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DESIGN OF A DIGITAL PHASE-LOCKED-LOOP CMOS UNIVERSAL ARRAY

R. H. Bergman, G. E. Skorup, and R. E. Funk
RCA Corporation
Solid State Division
Somerville, New Jersey 08876

PRRL-76-CR-54

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F33615-75-C-1252

FINAL REPORT
For the Period March 1975 to November 1976

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SEPTEMBER 1977

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Wright-Patterson AFB, Ohio 45433

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FOR THE COMMANDER

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Electronic Technology Division

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Metal-gate CMOS technology
TCC 051 universal array (UA)

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A digital phase-locked-loop circuit developed by The Charles Stark Draper Laboratory, Inc. and sponsored by the Air Force Avionics Laboratory, was successfully implemented on an RCA TCC 051 universal array (type number TCC 051 820).

Twenty engineering prototypes were evaluated by the contracting agency and found acceptable. An additional 150 units were subsequently supplied.

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20.

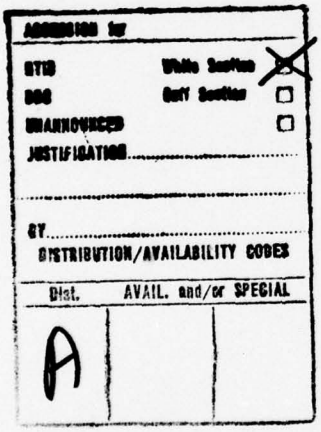
A market study was made of the commercial applicability of the DPLL LSI design.

PREFACE

This Final Report covers the work performed by the RCA Solid State Division, Somerville, New Jersey under Contract No. F33615-75-C-1252 during March 1975 through November 1976.

The Laboratory Director is G. B. Herzog, the Project Scientist is R. H. Bergman, and G. E. Skorup participated in the research. R. E. Funk did the market analysis.

This contract is being administered under the technical direction of G. Gaugler.



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SECTION I

OBJECTIVE

The hypha digital phase-locked loop (DPLL) makes possible a new method of phase processing which is easily implemented and which has many advantages over conventional methods of phase processing. The DPLL can perform narrow-bandwidth phase tracking with higher phase resolution than conventional integrated circuit analog phase-locked loops, which suffer from frequency instability of their voltage-controlled oscillators (VCC). The DPLL can also perform high-Q filtering, which is not possible with analog phase-locked loops.

Putting the DPLL on one integrated circuit would produce a functional module that would perform better and would be more easily utilized in many applications than the ones in which conventional PLL's are being used.

The objective of this program is to implement a DPLL circuit on a single large-scale-integration (LSI) chip by means of metal-gate CMOS technology.

SECTION II

SCOPE

This effort will provide the R&D required to fabricate prototype DPLL chips for test and evaluation in experimental communications and navigation circuitry.

SECTION III

WORK REQUIREMENTS/TASKS

A. IMPLEMENTATION

The design vehicle chosen to implement the digital phase-locked-loop logic is the TCC 051 universal array (UA). The TCC 051 universal array consists of PMOS devices, NMOS devices, p+ and n+ tunnels, zener diodes, and pads placed in a fixed pattern on a silicon substrate. All drains, sources, gates, tunnel ends, and pads are accessible for interconnection with metal. In the CMOS process, normally seven mask levels must be made for each design. In the UA technique, six of the seven mask layers are fixed for each array size. Only one mask level, the metal mask, is unique for each custom design. With this technique, a logic design engineer without semiconductor processing experience or knowledge of IC layout design rules can easily and readily originate his own, unique large-scale integrated circuit (LSI). A summary description of the array is given in Table 1.

TABLE 1. ARRAY SUMMARY DESCRIPTION

Title	Chip Size (mil)	No. of Internal Cells*	No. of Pads	No. of I/O Cells*	No. of High Z Cells*	No. of Low Z Cells*	Equiv. Cell Total*
TCC 051	229 x 232	240	48	24	8	4	276

*An equivalent cell consists of two p and two n devices.

Figure 1 shows a photograph of the array metal pattern form for the TCC 051. Actual size of the array layout form is 125 times actual chip size. At this scale, the grid line pattern has a grid spacing of 0.1 in., or 10 lines to the inch. The TCC 051 has 48 pads which are located around the periphery of the chip. Adjacent to each pad is a PMOS/NMOS pair which is normally connected to form an inverter for input wave shaping or for output buffering. Adjacent to these I/O devices and circling the internal-cell area are two concentric metal rings which are used for +V and -V supply voltage. In the center area of the array is a repeated pattern of internal cells which are

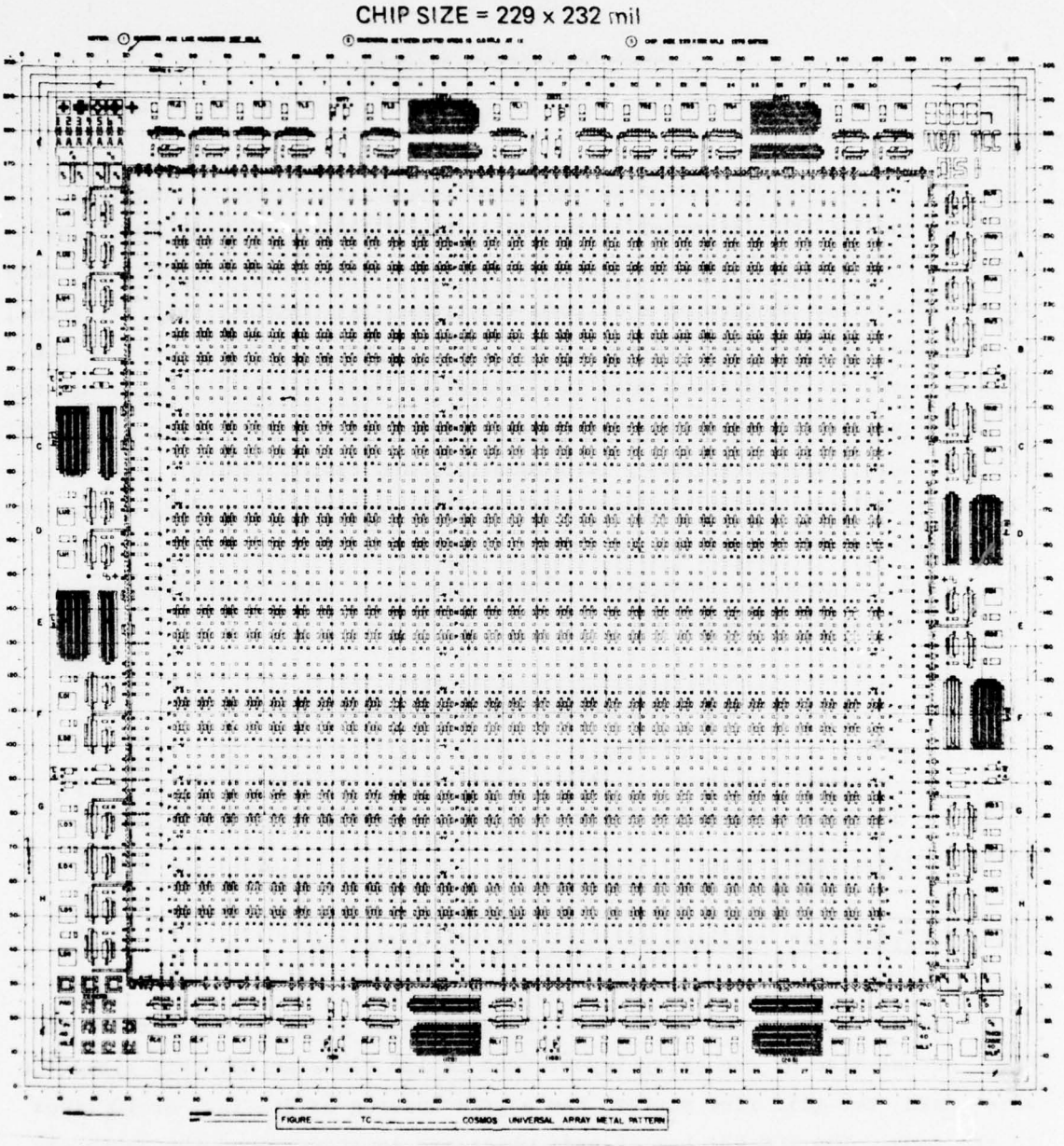


Figure 1. TCC 051 CMOS universal array metal pattern form.

used for the bulk of the logic. Additionally, eight pairs of very large devices can be seen in the periphery of the chip: two on each side. These are extra-large devices to be used for driving TTL and other off-chip devices requiring large sink/source currents. Also, four pairs of high-impedance devices are located on each of the four sides. These are useful for referencing floating input gates to either +V or -V. They may also be used as very slow inverters where long delay times are desired. In the lower left corner are located three large and eight small zener diodes for voltage regulation uses. In addition, there are various alignment marks and test devices for processing and control purposes.

A summary of the mask dimensions for the devices comprising each "cell type" is given in Table 2.

TABLE 2. ARRAY-DEVICE MASK SIZES

	p Device (mil)		n Device (mil)	
Cell Type	Width (W)	Length (L)*	Width (W)	Length (L)*
Internal	1.6	0.3	1.0	0.3
I/O	6.4	0.3	4.0	0.3
High Impedance	0.3	1.6	0.3	3.2
Low Impedance	54.4	0.3	28.8	0.3

*$\ell = L - 2\mu$

where ℓ = actual device channel length (mil)

L = mask dimension of device channel length (mil)

and μ = underdiffusion of drain and source into the channel area,

$\mu = 0.05 \pm 0.02$ mil.

E.g., for the nominal case, where

$L = 0.3$ mil and $\mu = 0.05$ mil

$\ell = L - 2\mu = 0.3 - 2(0.05) = 0.2$ mil.

A cross-section view of an internal cell (omitting tunnels) is shown in Fig. 2. Detailed layout and schematic information of the internal cell are

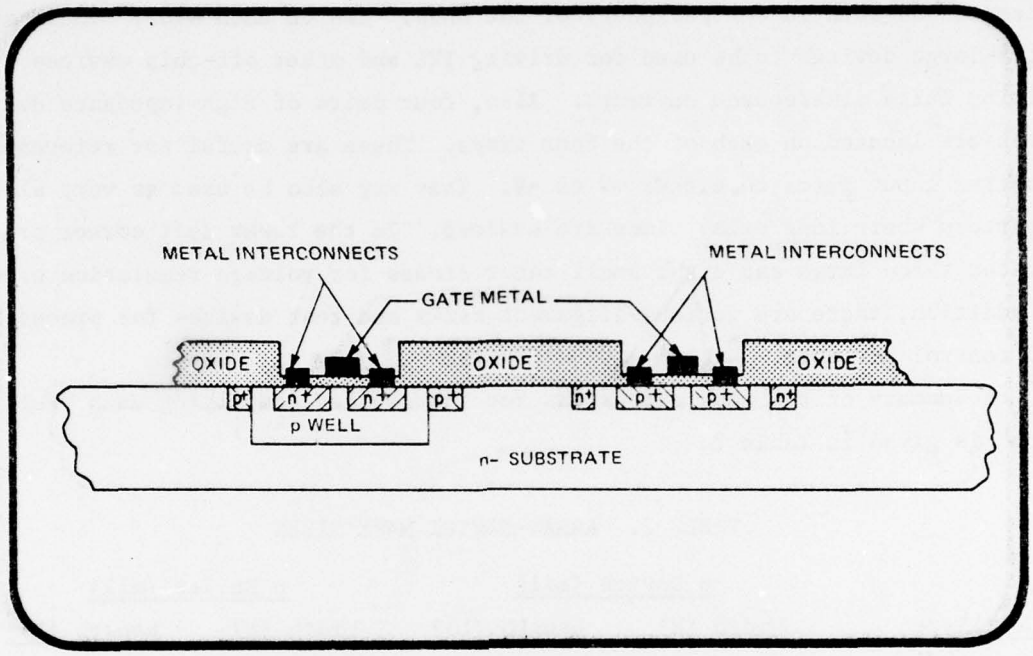


Figure 2. Internal-cell cross section.

shown in Fig. 3(a). Note that all drains, sources, tunnel ends, and +V and -V access areas occur at intersections of the 0.1-in. grid structure. Interconnection of access points to implement desired logic is made simply by drawing connecting lines with a layout pencil on the grid structure. Wherever a grid line occurs, it is a legitimate metal path. Actual grid spacing at chip level (1X) is 0.8 mil. Metal width is 0.4 mil. The uniform grid avoids any possibility of two metal paths being too close to one another. However, certain grid lines have been removed in some peripheral areas. *No metal run is allowed where the grid has been removed.* Second-level interconnect is provided by the fixed pattern of tunnels. Access to any tunnel is shown by a circle. Dashed lines indicate the inaccessible buried part of the tunnel.

Figure 3(b) shows the I/O cell and associated components such as pad, p+ protective diode, n+ protective diode, tunnels, and +V and -V bus runs. These components are used to implement the protected input circuit, as well as for output buffering and multiplexing outputs.

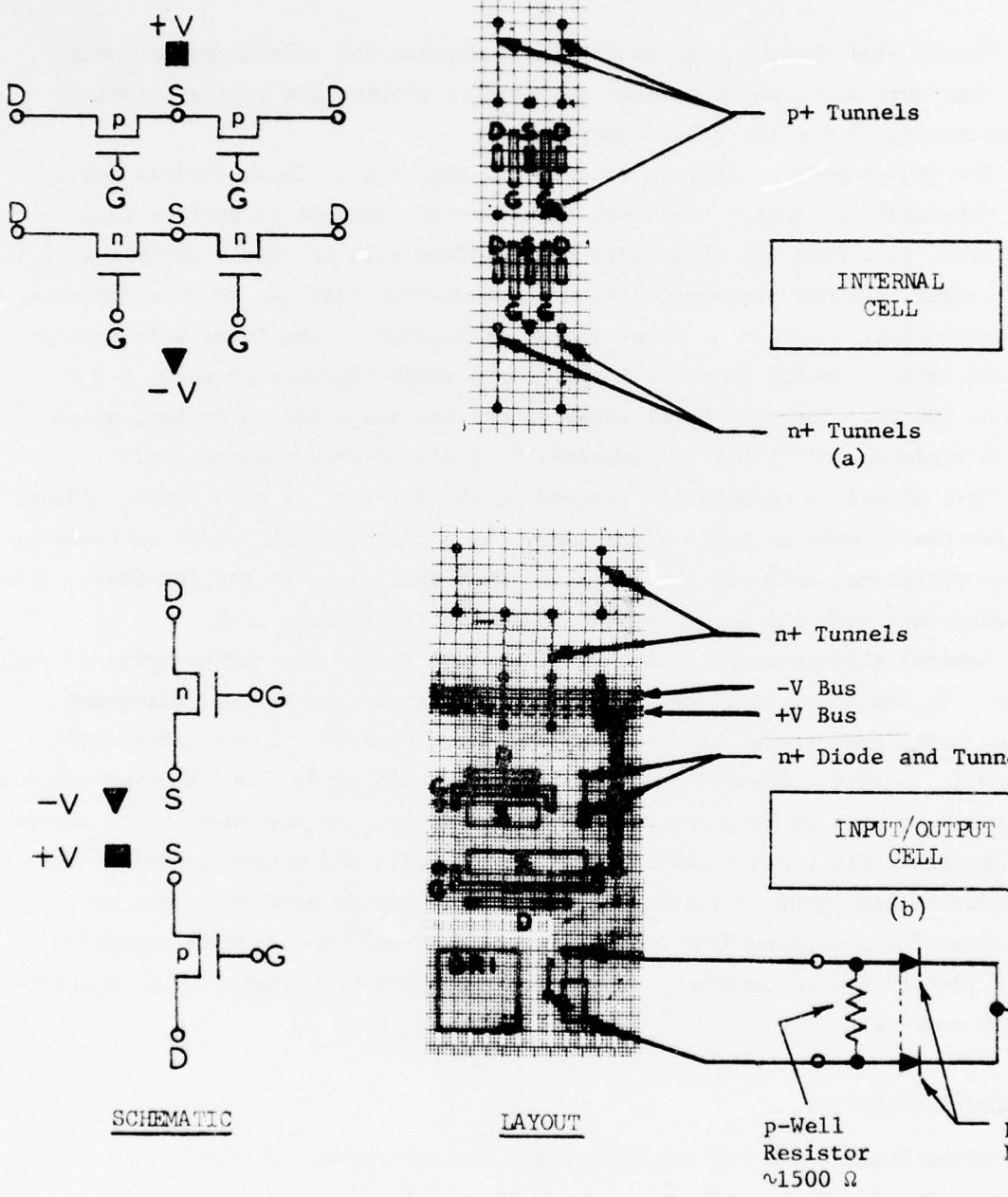


Figure 3. Internal and I/O layouts.

Figure 4(a) details the low-impedance devices and associated components. Note that very wide, short tunnels are used to provide low series impedance for accessing -V and the other runway area.

The high-impedance cell is detailed in Fig. 4(b). These devices may be used separately as active resistors or connected together to perform logic functions, just like the other cell types. This cell is particularly useful when larger internal propagation delays are desired than can be obtained with internal cells. A group of zener diodes is located in the lower left section of each array. There are three large zeners which regulate to about 5.5 V each at 100 μA. When all three large diodes are connected in series, an external resistance of 150 Ω is necessary to limit on-chip dissipation.

Both p+ and n+ tunnels are located in the interior of each array. Around the periphery, only n+ tunnels are used. As a consequence, tunnel resistances in the peripheral areas of the chip are lower than those of the interior. This is consistent with the lower device impedances in the same area.

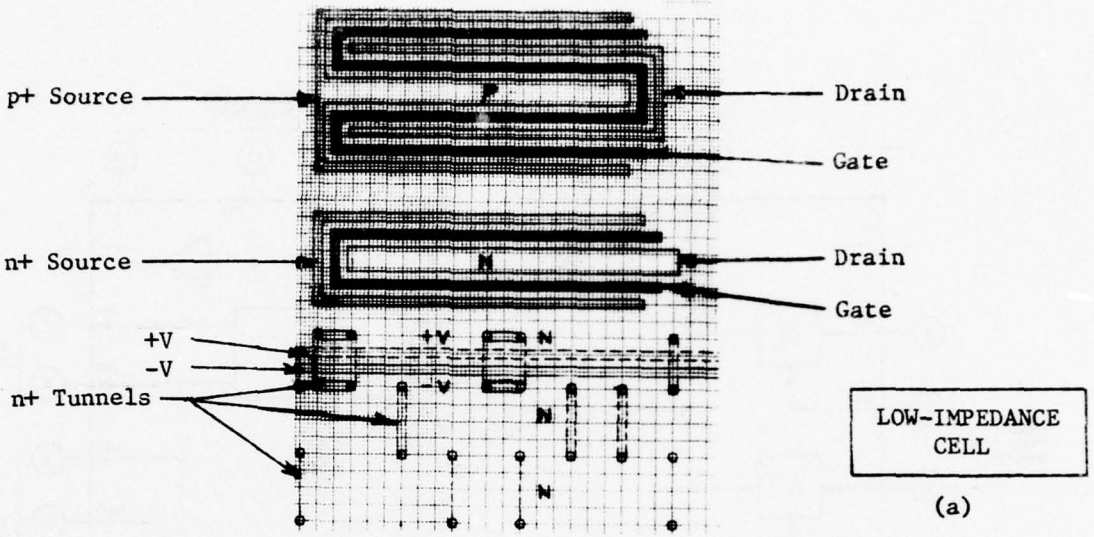
Several alignment and test devices are located in the corner areas of each array. In the upper left corner are located mask level-to-level alignment marks, level indicators, and 2-mil p and n test devices. In the lower left corner is located a 40-mil^2 area of metal over thin oxide (1000 Å) over original substrate to measure gate capacity of PMOS devices. In the lower right corner are located 4-mil p and n devices with 4-mil^2 drain and source areas for intermediate-level process testing, a 40-mil^2 thin-oxide capacitor over n+ substrate for measuring NMOS gate capacity, a 40-mil^2 thick-oxide capacitor, and a 10-mil^2 p-well resistor. The upper right corner contains chip identification numbers.

B. LOGIC SELECTION

Close liaison between the agency and the contractor defined the logic to be implemented. This is shown in block diagram form in Fig. 5.

C. LOGIC DESIGN AND MASK DEFINITION

Consultation on implementation of the logic design of the TCC 051 UA was initiated and continued until the total logic design was satisfactorily laid



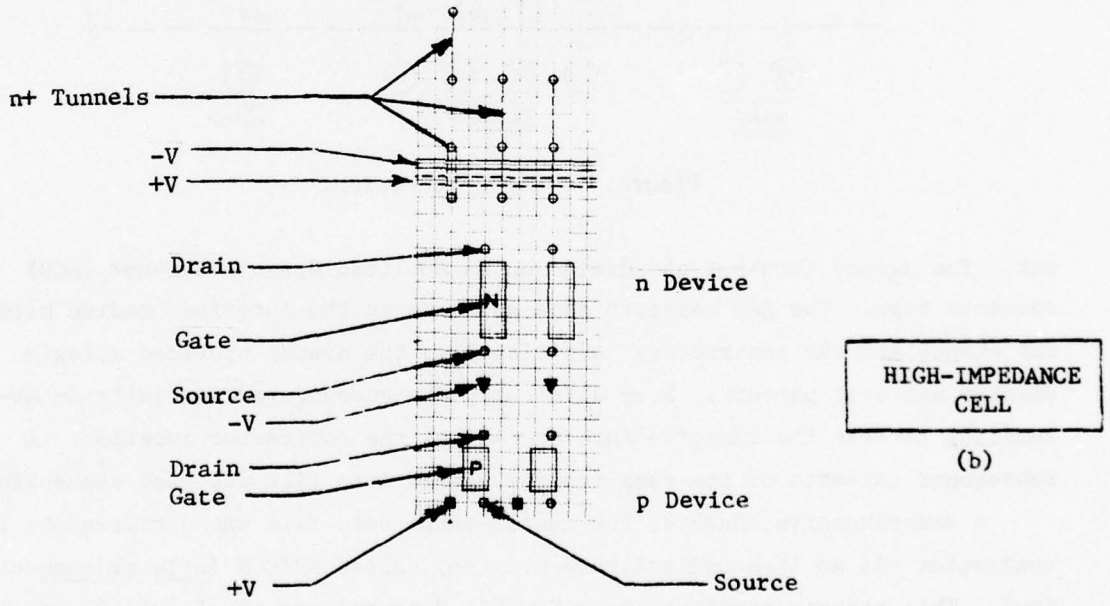


Figure 4. Low Z and high Z layouts.

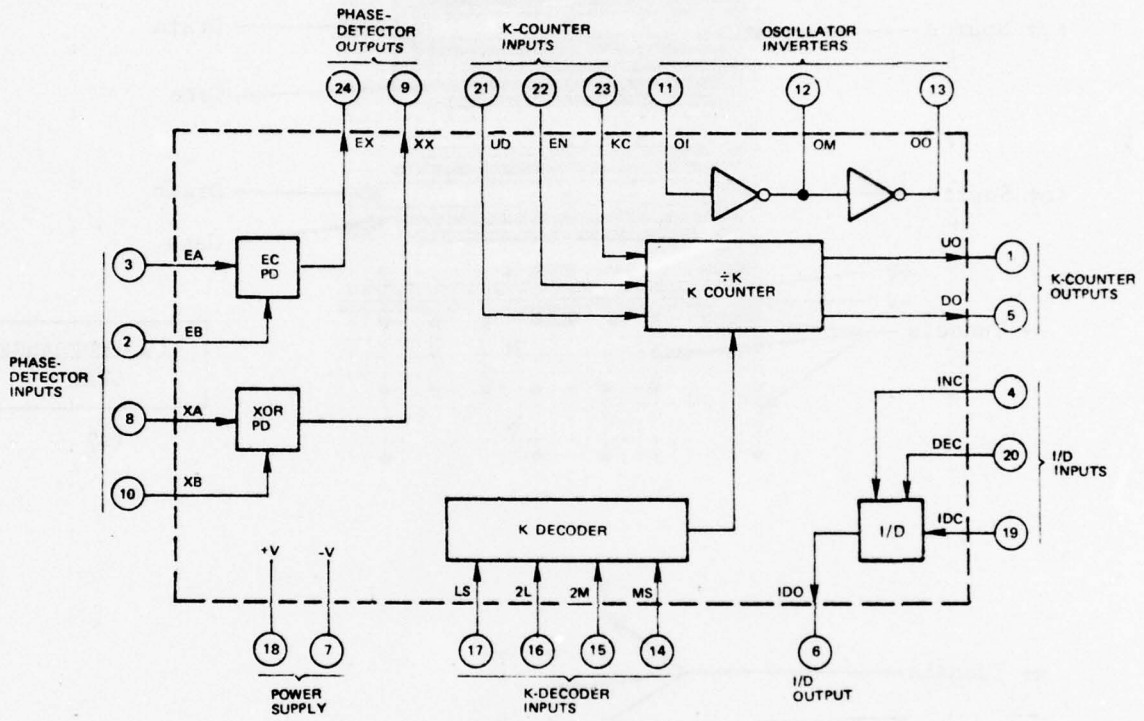


Figure 5. Logic selection.

out. The agency then put the design on an Applicon Graphic System* (AGS) cassette tape. The AGS cassette tape was used as the interface medium between the agency and the contractor. Additionally, the agency provided a logic diagram and test pattern. Some difficulty was encountered initially in attempting to read the cassette into the AGS at the contractor location. A subsequent cassette of the same (custom metal) data file was read successfully.

A comprehensive check of the custom-metal data file was performed by the contractor via an in-house software program, called ARTCON (artwork connectivity). This program combined basic TCC 051 data such as the locations of all drains, gates, sources, tunnel ends, and fixed metal with the custom-metal data and printed out a net list (Fig. 6). The net list contained the same information as was found in the logic diagram. The net list information was

*Registered trademark of Applicon Inc.

```
                                                                                00000010
                                                                                00000020
                                                                                00000030
    PROJ=0001                                                                   00000040
    PHY                                                                         00000050
(1) TYPE=C051 IPIN=RD5,LD3,LD5,BR1,BR6,TR3,TR5,RU5,RU3,LU6,LU4,LU2,BL6,TL5,$00000060
        TL4 OPIN=RD4,RD3,BL2,BR4,LD1,LD2,BL4,TL2,RU1,RD2,BR5,RU2,RD1,RD6,$ 00000070
        BL5 MPIN=TR1,BL1                                                        00000080
(2) PIN=LD3                                                                     00000090
    PIN=LD5                                                                     00000100
    PIN=LU6                                                                     00000110
    PIN=LU4                                                                     00000120
    PIN=RD4                                                                     00000130
    PIN=RD3                                                                     00000140
    PIN=BL2                                                                     00000150
    PIN=BR4                                                                     00000160
    PIN=LD1                                                                     00000170
    PIN=TR1                                                                     00000180
    PIN=BL1                                                                     00000190
                                                                                00000200
                                                                                00000210
    F PART= TYPE= FID=       ROT= I=  O=  M=                                    00000220
(3) 100     1950  X48Y299     2   NET-03847                                     $00000230
                                  100-NA                                        $00000240
                                  -                                              00000250
                                                                                 00000260
    101     1937  X6Y164      6   LU2                                           $00000270
                                  101-A,101-NA                                  $00000280
                                  -                                              00000290
    102     1950  X0Y151      6   101-NA                                        $00000300
                                  102-NA                                        $00000310
                                  -                                              00000320
    103     1948  X0Y214      6   100-NA,NET-03618                              $00000330
                                  103-X                                         $00000340
                                  -                                              00000350
    104     1948  X0Y239      6   NET-03618,NET-03847                           $00000360
                                  104-X                                         $00000370
                                  -                                              00000380
    105     1965  X90Y217     4   191-X,103-X                                   $00000390
                                  105-X                                         $00000400
                                  -                                              00000410
    106     1965  X79Y244     5   104-X,191-X                                   $00000420
                                  106-X                                         $00000430
                                  -                                              00000440
    107     1941  X93Y217     0   105-X,109-NB,101-NA,102-NA,102-NA,101-NA      $00000450
                                  107-X                                         $00000460
                                  -                                              00000470
    108     1941  X90Y244     2   110-NB,106-X,102-NA,101-NA,101-NA,102-NA      $00000480
                                  108-X                                         $00000490
                                  -                                              00000500
    109     1961  X100Y217    5   107-X,109-NA                                  $00000510
                                  109-NA,109-NB                                 $00000520
                                  -                                              00000530
    110     1961  X93Y244     0   108-X,110-NA                                  $00000540
                                  110-NA,110-NB                                 $00000550
```

1. Universal-array type and input and output pads used.
2. Pads with nonstandard I/O.
3. Connectivity data produced by ARTCON:
   e.g., Part number (PART=)
   Cell type (TYPE=)
   Cell location (FID=)
   Cell orientation (ROT=)
   Inputs (I=)
   Outputs (O=)
   Miscellaneous (M=)

Figure 6. ARTCON program output.

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compared, function for function and line for line, with the logic diagram. All was found to be correct. The custom-metal data file, therefore, was judged to be correct as received; it contains all the circuitry of the original logic diagram.

D. SIMULATION

Logic simulation and test generation were accomplished via the TGEN software program. ARTCON program output (Fig. 6) was used as the logic input to the simulation program. Some change in program format was made to TGEN compatibility. A printout of a portion of the simulation input to TGEN is shown in Fig. 7. Certain formating requirements of the TGEN require cell number assignments to differ from those originally used in the logic diagram.

Figure 8 shows a partial listing of these cross references. In addition to logic (Fig. 7) and cell cross-reference information (Fig. 8), the TGEN program required input stimuli to be specified. These were specified by the agency. The TGEN program then generated the test pattern shown in Fig. 9. Note that the first 15 columns contain the input signals. Columns 16 through 30 are test outputs. Columns 31 and 32 are +V and -V, respectively. Outputs obtained were compared against those predicted by the agency. Any discrepancies were resolved.

The final result was a test pattern that has been verified as being correct when applied to the logic that has been proven to be identical to that of the actual LSI chip.

E. SAMPLE FABRICATION

Artwork and masks were made from the verified custom-metal data file. These masks were applied to previously metallized wafers, which subsequently were tested against the test pattern of Fig. 9. Good chips were packaged and retested. Twenty of these working samples were sent to the agency for performance evaluations.

F. PROTOTYPE DEVICES

The working samples were evaluated by the agency and found to be completely satisfactory as received.

Subsequently to agency approval, 150 additional devices were delivered.

PR01	0002LC051		01/13/76		00000010
7	017	0	0		00000020
10	-2	1	108		00000030
11	-2	1	139		00000040
12	-2	1	205		00000050
13	-2	1	276		00000060
14	6	1	15		00000070
15	3	2	16	17	00000080
16	1	2	108	23	00000090
17	1	2	24	109	00000100
18	6	1	19		00000110
19	3	2	20	21	00000120
20	1	2	108	23	00000130
21	1	2	25	109	00000140
22	2	1	14		00000150
23	2	1	22		00000160
24	2	1	18		00000170
25	2	1	24		00000180
26	2	1	24		00000190
27	2	1	139		00000200
28	3	2	26	25	00000210
29	3	2	27	41	00000220
30	1	2	25	28	00000230
31	1	2	24	29	00000240
32	3	2	30	31	00000250
33	2	1	24		00000260
34	2	1	138		00000270
35	3	2	33	25	00000280
36	3	2	34	41	00000290
37	1	2	25	35	00000300
38	1	2	24	36	00000310
39	3	2	37	38	00000320
40	2	1	32		00000330
41	2	1	40		00000340
42	6	1	43		00000350
43	3	2	44	45	00000360
44	1	2	276	51	00000370
45	1	2	56	277	00000380
46	6	1	47		00000390
47	3	2	48	49	00000400
48	1	2	276	51	00000410
49	1	2	57	277	00000420
50	2	1	42		00000430
51	4	2	0	50	00000440
52	6	1	53		00000450
53	3	2	54	55	00000460
54	1	2	58	46	00000470
55	1	2	624	487	00000480
56	2	1	52		00000490
57	4	2	0	56	00000500
58	2	1	487		00000510
59	2	1	156		00000520
60	6	1	61		00000530
61	3	2	62	63	00000540
62	1	2	56	69	00000550

1. Number of inputs to circuit under test.
2. Total number of circuit elements.
3. Unique element name.
4. (-2) primary output identified by (-). Element type (2); e.g., NAND gate.
5. Number of inputs to element.
6. Element which drives the gate.

Figure 7. Simulators input (to TGEN).

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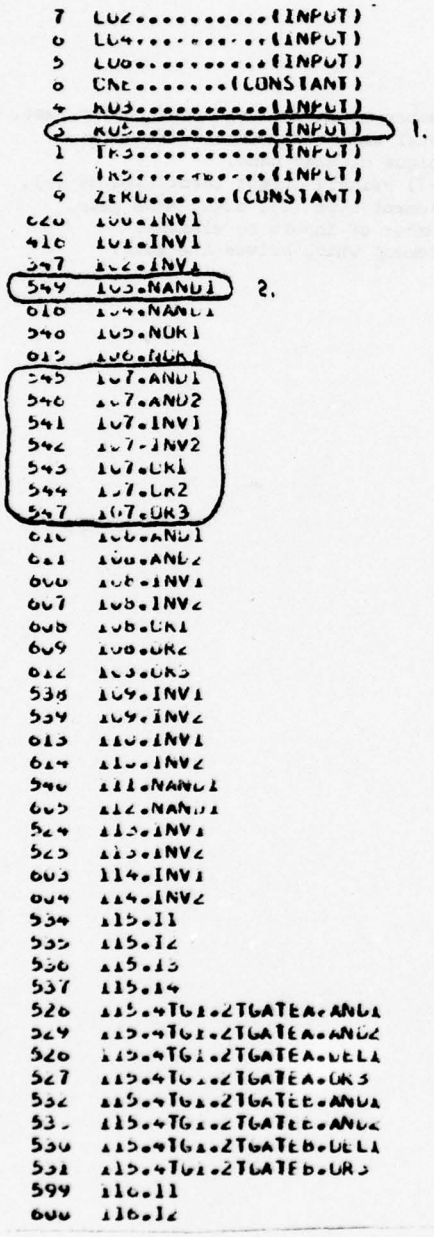

1. The IC input (RU5) is stimulated with the (3rd) input signal.
2. Layout cell (103), a NAND gate, is renamed element (549).
3. Layout cell (107), a transmission gate, is constructed from elements (541-547).

Figure 8. Cross reference between simulators, elements, and cells used during layout.

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		1 1 1 1 2 2 2 1 1 1 T T T T T T T T 3 1 1 1 7 6 5 4 1 2 3 3 2 4 0 9 8 0 1 P P P P 1 P P P P 5 1 6 9 2 3 8 7	
TEST	3	01001 10110 10011 00000 00000 00001 000	00000010
TEST	4	01001 11110 11011 00000 00000 00001 000	00000020
TEST	5	01001 10110 10011 00000 00000 01001 000	00000030
TEST	6	01001 00110 11011 00000 00000 01001 000	00000040
TEST	7	01001 01110 10011 00000 00000 00001 000	00000050
TEST	8	01001 00111 10011 00000 00000 00001 000	00000060
TEST	9	01001 10111 11011 00000 00000 00001 000	00000070
TEST	10	01001 11111 10011 00000 00000 01001 000	00000080
TEST	11	01001 10111 11011 10000 00000 01001 000	00000090
TEST	12	01001 11111 10011 10000 00000 00001 000	00000100
TEST	13	01001 10111 11011 10000 00000 01001 000	00000110
TEST	14	11001 10111 10011 10000 00000 00001 000	00000120
TEST	15	11001 11111 11011 10000 00000 01001 000	00000130
TEST	16	11001 10111 10011 00000 00000 00001 000	00000140
TEST	17	11001 11111 11011 00000 00000 00001 000	00000150
TEST	18	11001 10111 10011 10000 00000 01001 000	00000160
TEST	19	11001 11110 00011 10000 00000 01001 000	00000170
TEST	20	11001 10110 01011 00000 00000 01001 000	00000180
TEST	21	11001 11110 00011 00000 00000 00001 000	00000190
TEST	22	11001 10110 01011 10000 00000 00001 000	00000200
TEST	23	01001 10110 00011 10000 00000 00001 000	00000210
TEST	24	00001 10110 01011 10000 00000 00001 000	00000220
TEST	25	00101 10110 00011 10000 00000 00001 000	00000230
TEST	26	00101 11110 01011 10000 00000 00001 000	00000240
TEST	27	00101 10110 00011 00000 00000 01001 000	00000250
TEST	28	00101 11110 01011 00000 00000 01001 000	00000260
TEST	29	00101 10110 11011 00000 00000 01001 000	00000270
TEST	30	10101 10110 10011 00000 00000 00001 000	00000280
TEST	31	10101 11110 11011 00000 00000 00001 000	00000290
TEST	32	10101 10110 10011 01000 00000 01001 000	00000300
TEST	33	10101 11110 11011 01000 00000 01001 000	00000310
TEST	34	10101 10110 10011 01000 00000 00001 000	00000320
TEST	35	00101 10111 00011 01000 00000 00001 000	00000330
TEST	36	01101 10111 01011 01000 00000 00001 000	00000340
TEST	37	01101 11111 00011 01000 00000 01001 000	00000350
TEST	38	01101 10111 01011 10000 00000 01001 000	00000360
TEST	39	01101 11111 00011 10000 00000 00001 000	00000370
TEST	40	01101 10111 01011 10000 00000 00001 000	00000380
TEST	41	01101 11111 00011 10000 00000 01001 000	00000390
TEST	42	01101 10111 01011 01000 00000 01001 000	00000400
TEST	43	01101 11111 00011 01000 00000 00001 000	00000410
TEST	44	01101 10110 10011 01000 00000 00001 000	00000420
TEST	45	11101 10110 11011 11000 00000 00001 000	00000430
TEST	46	11101 11110 10011 11000 00000 01001 000	00000440
TEST	47	11101 10110 11011 00000 00000 01001 000	00000450
TEST	48	11101 11110 10011 00000 00000 00001 000	00000460
TEST	49	11101 10110 11011 11000 00000 00001 000	00000470
TEST	50	11101 11110 10011 11000 00000 01001 000	00000480
TEST	51	11101 10110 10011 00000 00000 01001 000	00000490
TEST	52	11101 11110 10011 00000 00000 01001 000	00000500
TEST	53	11101 10110 10011 11000 00000 01001 000	00000510
TEST	54	11101 11110 10011 11000 00000 01001 000	00000520
TEST	55	11101 10110 10011 00000 00000 01001 000	00000530
TEST	56	11101 11110 10011 00000 00000 01001 000	00000540
TEST	57	11101 10110 10011 11000 00000 01001 000	00000550

1. IC package pin numbers as per the DPLL block diagram (Fig. 5). TP denotes test points that are used at wafer test and not wired to socket pins.
2. Test patterns generated by simulator and used for functional testing.

Figure 9. Simulator (TGEN) output.

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```
TEST   58    11101 11110 10011 11000 00000 01001 000    00000560
TEST   59    11101 10110 10011 00000 00000 01001 000    00000570
TEST   60    11101 11110 10011 00000 00000 01001 000    00000580
TEST   61    11101 10110 10011 11000 00000 01001 000    00000590
TEST   62    01101 10110 10011 11000 00000 01001 000    00000600
TEST   63    00101 10110 10011 11000 00000 01001 000    00000610
TEST   64    00101 11110 10011 11000 00000 01001 000    00000620
TEST   65    00101 10110 10011 00000 00000 01001 000    00000630
TEST   66    00101 11110 10011 00000 00000 01001 000    00000640
TEST   67    00101 10110 10011 00000 00000 01001 000    00000650
TEST   68    00101 11110 10011 00000 00000 01001 000    00000660
TEST   69    00101 10110 10011 00000 00000 01001 000    00000670
TEST   70    00101 11110 10011 00000 00000 01001 000    00000680
TEST   71    00101 10110 10011 00000 00000 01001 000    00000690
TEST   72    00101 11110 10011 00000 00000 01001 000    00000700
TEST   73    00101 10110 10011 10000 00000 01001 000    00000710
TEST   74    00101 11110 10011 10000 00000 01001 000    00000720
TEST   75    00101 10110 10011 10000 00000 01001 000    00000730
TEST   76    00101 11110 10011 10000 00000 01001 000    00000740
TEST   77    00101 10110 10011 10000 00000 01001 000    00000750
TEST   78    00101 11110 10011 10000 00000 01001 000    00000760
TEST   79    00101 10110 10011 10000 00000 01001 000    00000770
TEST   80    00001 10110 10011 10000 00000 01001 000    00000780
TEST   81    00011 10110 10011 10000 00000 01001 000    00000790
TEST   82    00011 11110 10011 10000 00000 01001 000    00000800
TEST   83    00011 10110 10011 01100 00000 01001 000    00000810
TEST   84    00011 11110 10011 01100 00000 01001 000    00000820
TEST   85    00011 10110 10011 01100 00000 01001 000    00000830
TEST   86    00011 11110 10011 01100 00000 01001 000    00000840
TEST   87    00011 10110 10011 01100 00000 01001 000    00000850
TEST   88    00011 11110 10011 01100 00000 01001 000    00000860
TEST   89    00011 10110 10011 01100 00000 01001 000    00000870
TEST   90    00011 11110 10011 01100 00000 01001 000    00000880
TEST   91    00011 10110 10011 11100 00000 01001 000    00000890
TEST   92    00011 11110 10011 11100 00000 01001 000    00000900
TEST   93    00011 10110 10011 11100 00000 01001 000    00000910
TEST   94    10011 10110 10011 11100 00000 01001 000    00000920
TEST   95    10011 11110 10011 11100 00000 01001 000    00000930
TEST   96    10011 10110 10011 11000 00000 01001 000    00000940
TEST   97    10011 11110 10011 11000 00000 01001 000    00000950
TEST   98    10011 10110 10011 11000 00000 01001 000    00000960
TEST   99    00011 10110 10011 11000 00000 01001 000    00000970
TEST  100    01011 10110 10011 11000 00000 01001 000    00000980
TEST  101    01011 11110 10011 11000 00000 01001 000    00000990
TEST  102    01011 10110 10011 01100 00000 01001 000    00001000
TEST  103    01011 11110 10011 01100 00000 01001 000    00001010
TEST  104    01011 10110 10011 01100 00000 01001 000    00001020
TEST  105    01011 11110 10011 01100 00000 01001 000    00001030
TEST  106    01011 10110 10011 11000 00000 01001 000    00001040
TEST  107    01011 11110 10011 11000 00000 01001 000    00001050
TEST  108    01011 10110 10011 11000 00000 01001 000    00001060
TEST  109    11011 10110 10011 11100 00000 01001 000    00001070
TEST  110    11011 11110 10011 11100 00000 01001 000    00001080
TEST  111    11011 10110 10011 01000 00000 01001 000    00001090
TEST  112    11011 11110 10011 01000 00000 01001 000    00001100
```

Figure 9. Continued.

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```
TEST  113   11011 10110 10011 11100 00000 01001 000   00001110
TEST  114   11011 11110 10011 11100 00000 01001 000   00001120
TEST  115   11011 10110 10011 01000 00000 01001 000   00001130
TEST  116   11011 11110 10011 01000 00000 01001 000   00001140
TEST  117   11011 10110 10011 11100 00000 01001 000   00001150
TEST  118   11011 11110 10011 11100 00000 01001 000   00001160
TEST  119   11011 10110 10011 01000 00000 01001 000   00001170
TEST  120   11011 11110 10011 01000 00000 01001 000   00001180
TEST  121   11011 10110 10011 11100 00000 01001 000   00001190
TEST  122   11011 11110 10011 11100 00000 01001 000   00001200
TEST  123   11011 10110 10011 01000 00000 01001 000   00001210
TEST  124   11011 11110 10011 01000 00000 01001 000   00001220
TEST  125   11011 10110 10011 11100 00000 01001 000   00001230
TEST  126   01011 10110 10011 11100 00000 01001 000   00001240
TEST  127   00011 10110 10011 11100 00000 01001 000   00001250
TEST  128   00111 10110 10011 11100 00000 01001 000   00001260
TEST  129   00111 11110 10011 11100 00000 01001 000   00001270
TEST  130   00111 10110 10011 01110 00000 01001 000   00001280
TEST  131   00111 11110 10011 01110 00000 01001 000   00001290
TEST  132   00111 10110 10011 01110 00000 01001 000   00001300
TEST  133   10111 10110 10011 01110 00000 01001 000   00001310
TEST  134   10111 11110 10011 01110 00000 01001 000   00001320
TEST  135   10111 10110 10011 01110 00000 01001 000   00001330
TEST  136   10111 11110 10011 01110 00000 01001 000   00001340
TEST  137   10111 10110 10011 01110 00000 01001 000   00001350
TEST  138   10111 11110 10011 01110 00000 01001 000   00001360
TEST  139   10111 10110 10011 11100 00000 01001 000   00001370
TEST  140   10111 11110 10011 11100 00000 01001 000   00001380
TEST  141   10111 10110 10011 11100 00000 01001 000   00001390
TEST  142   00111 10110 10011 11100 00000 01001 000   00001400
TEST  143   01111 10110 10011 11100 00000 01001 000   00001410
TEST  144   01111 11110 10011 11100 00000 01001 000   00001420
TEST  145   01111 10110 10011 01110 00000 01001 000   00001430
TEST  146   01111 11110 10011 01110 00000 01001 000   00001440
TEST  147   01111 10110 10011 01110 00000 01001 000   00001450
TEST  148   01111 11110 10011 01110 00000 01001 000   00001460
TEST  149   01111 10110 10011 11101 00000 01001 000   00001470
TEST  150   01111 11110 10011 11101 00000 01001 000   00001480
TEST  151   01111 10110 10011 11101 00000 01001 000   00001490
TEST  152   11111 10110 10011 11111 00000 01001 000   00001500
TEST  153   11111 11110 10011 11111 00000 01001 000   00001510
TEST  154   11111 10110 10011 00001 00000 01001 000   00001520
TEST  155   11111 11110 10011 00001 00000 01001 000   00001530
TEST  156   11111 10110 10011 10011 00000 01001 000   00001540
TEST  157   11111 11110 10011 10011 00000 01001 000   00001550
TEST  158   11111 10110 10011 00000 00000 01001 000   00001560
TEST  159   11111 11110 10011 00000 00000 01001 000   00001570
TEST  160   11111 10110 10011 10010 00000 01001 000   00001580
TEST  161   11111 11110 10011 10010 00000 01001 000   00001590
TEST  162   11111 10110 10011 00000 00000 01001 000   00001600
TEST  163   01000 10110 10011 00000 00000 01001 000   00001610
TEST  164   01000 11110 10011 00000 00000 01001 000   00001620
TEST  165   01000 10110 10011 00000 00000 01001 000   00001630
TEST  166   01000 00110 10011 00000 00000 01001 000   00001640
TEST  167   01000 01110 10011 00000 00000 01001 000   00001650
```

Figure 9. Continued.

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```
TEST  168   01000 00110 10011 00000 00000 01001 000   00001660
TEST  169   01000 10110 10011 00000 00000 01001 000   00001670
TEST  170   01000 11110 10011 00000 00000 01001 000   00001680
TEST  171   01000 10110 10011 00000 10000 01001 000   00001690
TEST  172   01000 11110 10011 00000 10000 01001 000   00001700
TEST  173   01000 10110 10011 00000 10000 01001 000   00001710
TEST  174   11000 10110 10011 00000 10000 01001 000   00001720
TEST  175   11000 11110 10011 00000 10000 01001 000   00001730
TEST  176   11000 10110 10011 00000 00000 01001 000   00001740
TEST  177   11000 11110 10011 00000 00000 01001 000   00001750
TEST  178   11000 10110 10011 00000 10000 01001 000   00001760
TEST  179   11000 11110 10011 00000 10000 01001 000   00001770
TEST  180   11000 10110 10011 00000 00000 01001 000   00001780
TEST  181   11000 11110 10011 00000 00000 01001 000   00001790
TEST  182   11000 10110 10011 00000 10000 01001 000   00001800
TEST  183   01000 10110 10011 00000 10000 01001 000   00001810
TEST  184   00000 10110 10011 00000 10000 01001 000   00001820
TEST  185   00100 10110 10011 00000 10000 01001 000   00001830
TEST  186   00100 11110 10011 00000 10000 01001 000   00001840
TEST  187   00100 10110 10011 00000 00000 01001 000   00001850
TEST  188   00100 11110 10011 00000 00000 01001 000   00001860
TEST  189   00100 10110 10011 00000 00000 01001 000   00001870
TEST  190   10100 10110 10011 00000 00000 01001 000   00001880
TEST  191   10100 11110 10011 00000 00000 01001 000   00001890
TEST  192   10100 10110 10011 00000 01000 01001 000   00001900
TEST  193   10100 11110 10011 00000 01000 01001 000   00001910
TEST  194   10100 10110 10011 00000 01000 01001 000   00001920
TEST  195   00100 10110 10011 00000 01000 01001 000   00001930
TEST  196   01100 10110 10011 01000 01000 01001 000   00001940
TEST  197   01100 11110 10011 01000 01000 01001 000   00001950
TEST  198   01100 10110 10011 01000 10000 01001 000   00001960
TEST  199   01100 11110 10011 01000 10000 01001 000   00001970
TEST  200   01100 10110 10011 01000 10000 01001 000   00001980
TEST  201   01100 11110 10011 01000 10000 01001 000   00001990
TEST  202   01100 10110 10011 01000 01000 01001 000   00002000
TEST  203   01100 11110 10011 01000 01000 01001 000   00002010
TEST  204   01100 10110 10011 01000 01000 01001 000   00002020
TEST  205   11100 10110 10011 00000 11000 01001 000   00002030
TEST  206   11100 11110 10011 00000 11000 01001 000   00002040
TEST  207   11100 10110 10011 00000 00000 01001 000   00002050
TEST  208   11100 11110 10011 00000 00000 01001 000   00002060
TEST  209   11100 10110 10011 00000 11000 01001 000   00002070
TEST  210   11100 11110 10011 00000 11000 01001 000   00002080
TEST  211   11100 10110 10011 00000 00000 01001 000   00002090
TEST  212   11100 11110 10011 00000 00000 01001 000   00002100
TEST  213   11100 10110 10011 00000 11000 01001 000   00002110
TEST  214   11100 11110 10011 00000 11000 01001 000   00002120
TEST  215   11100 10110 10011 00000 00000 01001 000   00002130
TEST  216   11100 11110 10011 00000 00000 01001 000   00002140
TEST  217   11100 10110 10011 00000 11000 01001 000   00002150
TEST  218   11100 11110 10011 00000 11000 01001 000   00002160
TEST  219   11100 10110 10011 00000 00000 01001 000   00002170
TEST  220   11100 11110 10011 00000 00000 01001 000   00002180
TEST  221   11100 10110 10011 00000 11000 01001 000   00002190
TEST  222   01100 10110 10011 01000 11000 01001 000   00002200
```

Figure 9. Continued.

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```
TEST  223   00100 10110 10011 01000 11000 01001 000   00002210
TEST  224   00100 11110 10011 01000 11000 01001 000   00002220
TEST  225   00100 10110 10011 01000 00000 01001 000   00002230
TEST  226   00100 11110 10011 01000 00000 01001 000   00002240
TEST  227   00100 10110 10011 01000 00000 01001 000   00002250
TEST  228   00100 11110 10011 01000 00000 01001 000   00002260
TEST  229   00100 10110 10011 01000 00000 01001 000   00002270
TEST  230   00100 11110 10011 01000 00000 01001 000   00002280
TEST  231   00100 10110 10011 01000 00000 01001 000   00002290
TEST  232   00100 11110 10011 01000 00000 01001 000   00002300
TEST  233   00100 10110 10011 01000 10000 01001 000   00002310
TEST  234   00100 11110 10011 01000 10000 01001 000   00002320
TEST  235   00100 10110 10011 01000 10000 01001 000   00002330
TEST  236   00100 11110 10011 01000 10000 01001 000   00002340
TEST  237   00100 10110 10011 01000 10000 01001 000   00002350
TEST  238   00100 11110 10011 01000 10000 01001 000   00002360
TEST  239   00100 10110 10011 01000 10000 01001 000   00002370
TEST  240   00000 10110 10011 01000 10000 01001 000   00002380
TEST  241   00010 10110 10011 01000 10000 01001 000   00002390
TEST  242   00010 11110 10011 01000 10000 01001 000   00002400
TEST  243   00010 10110 10011 01000 01100 01001 000   00002410
TEST  244   00010 11110 10011 01000 01100 01001 000   00002420
TEST  245   00010 10110 10011 01000 01100 01001 000   00002430
TEST  246   00010 11110 10011 01000 01100 01001 000   00002440
TEST  247   00010 10110 10011 01000 01100 01001 000   00002450
TEST  248   00010 11110 10011 01000 01100 01001 000   00002460
TEST  249   00010 10110 10011 01000 01100 01001 000   00002470
TEST  250   00010 11110 10011 01000 01100 01001 000   00002480
TEST  251   00010 10110 10011 01000 11100 01001 000   00002490
TEST  252   00010 11110 10011 01000 11100 01001 000   00002500
TEST  253   00010 10110 10011 01000 11100 01001 000   00002510
TEST  254   10010 10110 10011 01000 11100 01001 000   00002520
TEST  255   10010 11110 10011 01000 11100 01001 000   00002530
TEST  256   10010 10110 10011 01000 11000 01001 000   00002540
TEST  257   10010 11110 10011 01000 11000 01001 000   00002550
TEST  258   10010 10110 10011 01000 11000 01001 000   00002560
TEST  259   00010 10110 10011 01000 11000 01001 000   00002570
TEST  260   01010 10110 10011 01100 11000 01001 000   00002580
TEST  261   01010 11110 10011 01100 11000 01001 000   00002590
TEST  262   01010 10110 10011 01100 01100 01001 000   00002600
TEST  263   01010 11110 10011 01100 01100 01001 000   00002610
TEST  264   01010 10110 10011 01100 01100 01001 000   00002620
TEST  265   01010 11110 10011 01100 01100 01001 000   00002630
TEST  266   01010 10110 10011 01100 11000 01001 000   00002640
TEST  267   01010 11110 10011 01100 11000 01001 000   00002650
TEST  268   01010 10110 10011 01100 11000 01001 000   00002660
TEST  269   11010 10110 10011 01000 11100 01001 000   00002670
TEST  270   11010 11110 10011 01000 11100 01001 000   00002680
TEST  271   11010 10110 10011 01000 01000 01001 000   00002690
TEST  272   11010 11110 10011 01000 01000 01001 000   00002700
TEST  273   11010 10110 10011 01000 11100 01001 000   00002710
TEST  274   11010 11110 10011 01000 11100 01001 000   00002720
TEST  275   11010 10110 10011 01000 01000 01001 000   00002730
TEST  276   11010 11110 10011 01000 01000 01001 000   00002740
TEST  277   11010 10110 10011 01000 11100 01001 000   00002750
```

Figure 9. Continued.

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```
TEST  278   11010 11110 10011 01000 11100 01001 000   00002760
TEST  279   11010 10110 10011 01000 01000 01001 000   00002770
TEST  280   11010 11110 10011 01000 01000 01001 000   00002780
TEST  281   11010 10110 10011 01000 11100 01001 000   00002790
TEST  282   11010 11110 10011 01000 11100 01001 000   00002800
TEST  283   11010 10110 10011 01000 01000 01001 000   00002810
TEST  284   11010 11110 10011 01000 01000 01001 000   00002820
TEST  285   11010 10110 10011 01000 11100 01001 000   00002830
TEST  286   01010 10110 10011 01100 11100 01001 000   00002840
TEST  287   00010 10110 10011 01100 11100 01001 000   00002850
TEST  288   00110 10110 10011 01100 11100 01001 000   00002860
TEST  289   00110 11110 10011 01100 11100 01001 000   00002870
TEST  290   00110 10110 10011 01100 01110 01001 000   00002880
TEST  291   00110 11110 10011 01100 01110 01001 000   00002890
TEST  292   00110 10110 10011 01100 01110 01001 000   00002900
TEST  293   10110 10110 10011 01110 01110 01001 000   00002910
TEST  294   10110 11110 10011 01110 01110 01001 000   00002920
TEST  295   10110 10110 10011 01110 01110 01001 000   00002930
TEST  296   10110 11110 10011 01110 01110 01001 000   00002940
TEST  297   10110 10110 10011 01110 01110 01001 000   00002950
TEST  298   10110 11110 10011 01110 01110 01001 000   00002960
TEST  299   10110 10110 10011 01110 11100 01001 000   00002970
TEST  300   10110 11110 10011 01110 11100 01001 000   00002980
TEST  301   10110 10110 10011 01110 11100 01001 000   00002990
TEST  302   00110 10110 10011 01110 11100 01001 000   00003000
TEST  303   01110 10110 10011 01110 11100 01001 000   00003010
TEST  304   01110 11110 10011 01110 11100 01001 000   00003020
TEST  305   01110 10110 10011 01110 01110 01001 000   00003030
TEST  306   01110 11110 10011 01110 01110 01001 000   00003040
TEST  307   01110 10110 10011 01110 01110 01001 000   00003050
TEST  308   01110 11110 10011 01110 01110 01001 000   00003060
TEST  309   01110 10110 10011 11110 11101 01001 000   00003070
TEST  310   01110 11110 10011 11110 11101 01001 000   00003080
TEST  311   01110 10110 10011 11110 11101 01001 000   00003090
TEST  312   11110 10110 10011 11101 11111 01001 000   00003100
TEST  313   11110 11110 10011 11101 11111 01001 000   00003110
TEST  314   11110 10110 10011 11101 00001 01001 000   00003120
TEST  315   11110 11110 10011 11101 00001 01001 000   00003130
TEST  316   11110 10110 10011 11101 10011 01001 000   00003140
TEST  317   11110 11110 10011 11101 10011 01001 000   00003150
TEST  318   11110 10110 10011 01101 00000 01001 000   00003160
TEST  319   11110 11110 10011 01101 00000 01001 000   00003170
TEST  320   11110 10110 10011 01101 10010 01001 000   00003180
TEST  321   11110 11110 10011 01101 10010 01001 000   00003190
TEST  322   11110 10110 10011 01101 00000 01001 000   00003200
```

Figure 9. Continued.

G. APPLICATIONS STUDY

An applications study of the market for DPLL devices was made and is presented in the Appendix.

H. RELIABILITY

The following reliability prediction presents estimates on CMOS devices made by RCA. Table 3 shows a reliability prediction at three temperatures

(125, -55, and 25°C) for products made in 1972; the calculated reliability figures represent 1122 parts operating for 1000 h each, the median operating time for each part. Table 3 also presents similar predicted reliability on CMOS parts operated 24,000 h each, with approximately three years' continuous operation at 125°C. The calculated values in Table 3 are representative of the reliability that could be expected from parts used in the digital timer.

TABLE 3. CMOS HIGH-RELIABILITY DATA

Device Tested	CD 4000 Family†	CD 4001 D††	
No. in Sample	1122	75	
Specification Data Sheet	TIC-102 (MIL-STD-883, method 5004)	TIC-101A, temp range: -55 to +125°C	
Test Hours	1000*	24,000 (May 1973)	
Total Device Hours	1,055,372	1,784,000	
Inoperable Failures	zero	zero	
125°C Failure Rate (%/1000 h)	0.086	0.051	
-55°C Failure Rate (%/1000 h)**	0.0126	0.0075	at 60% Confidence
25°C Failure Rate (%/1000 h)**	0.0037	0.0022	at 60% Confidence

*Of these, 231 units had less than 1000 h.

**Using accelerating factors from 125°C.

†These data provide a summary of group B (MIL-STD-883) 125°C operating-life data for 1972 on RCA high-reliability parts. The parts were processed per RCA level 2. The data, then, are representative of the life capability of 1972 shipments of CMOS high-reliability parts.

††This sample has been operating continually at 125°C since 1970 in a ring-counter application which exercises the circuits in a functional mode. The units are still under test. This indicates the long-term reliability of CMOS circuits.

SECTION IV

RESULTS AND CONCLUSIONS

The DPLL design was successfully implemented on the TCC 051 universal array. Interfacing between the agency and contractor was successfully accomplished via an AGS cassette. Tests made by the contractor showed that the design performed as well as or better than expected. No corrections for errors were necessary; the very first units fabricated operated as predicted.

APPENDIX

DIGITAL PHASE-LOCKED-LOOP APPLICATIONS STUDY

A. INTRODUCTION

C. S. Draper Labs has reported [1] a new all-digital PLL. Based on a straightforward digital design approach, this PLL has advantages over other more complicated PLL's, as well as over the widely used analog PLL's. Because of the increasing emphasis on digital circuitry to decrease cost, increase reliability, reduce size, and obtain freedom from "analog" drift, there is an increasing effort to develop digital phase-locked-loop (DPLL) circuits.

RCA Solid State Technology Center has implemented the basic C. S. Draper Labs DPLL with a CMOS universal array [2].

This report discusses the characteristics as well as the military and commercial applications of the DPLL, drawing on the PLL experience of the RCA Solid State Division CMOS Applications Department, the literature, and the author's experience with PLL's. The range of applications discussed does not differentiate between commercial and military markets, but clearly can and does include both.

The DPLL is compared with widely applied analog PLL IC's to show advantages and disadvantages. No attempt is being made to cover a complete range of analog, analog-digital (hybrid), and discrete PLL's, of arithmetic synthesizers, and of other DPLL forms as reported by S. Gupta [3] and others.

B. ANALOG AND DIGITAL PLL's: ARCHITECTURE AND PROPERTIES

Properties and characteristics of analog and digital PLL's are briefly defined; both first- and second-order-type loops are shown with both analog and digital approaches.

Figure A-1 is a block diagram of a first-order PLL consisting of a phase detector and VCO function. Depending on application, outputs are either at the phase detector (ϕ) for demodulation, or at the VCO output for frequency tracking, synchronization, filtering, etc.

---

1. W. Lee, E. Harrington, and D. Cox, *A New IC Digital PLL*, Draper Laboratory Report, P-148, March 1975.
2. R. Horton, *The Development of a DPLL IC*, Draper Laboratory Report, P-272, April 1976.
3. S. Gupta, "Phase-Locked Loops," Proc. IEEE, 63, No. 2, Feb. 1975.

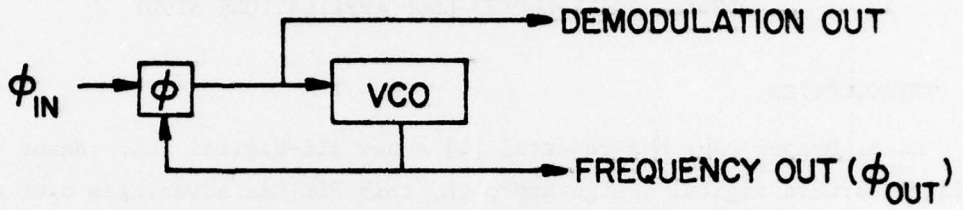

Figure A-1. First-order PLL.

Note that for the first-order PLL there is no loop filter; this results in a loop with an inherent incremental-step frequency error and a lock range limited by the phase detector and VCO gain constraints, i.e., a limited lock-range capability.

Figure A-2 is a second-order PLL where a loop filter enhances loop operation.

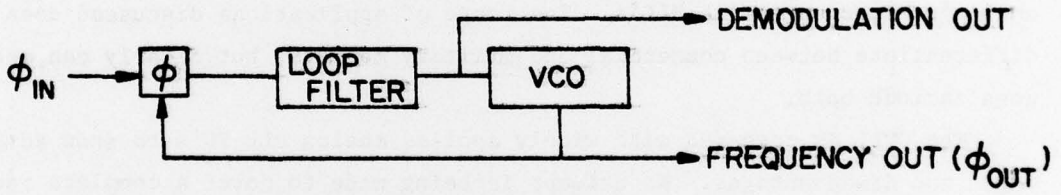

Figure A-2. Second-order PLL.

Use of an "ideal" loop filter results in a theoretically "pure" integrator and produces zero loop phase error as well as zero frequency step error. The pull-in range is theoretically infinite; in most narrow-band, high-Q applications of PLL's second-order loops are used.

"Ideal Filter" - A type II loop is most popular because the phase step error ($\theta i(t)$) is equal to zero and the frequency step error, $\phi i(t) = \omega \Delta t + \theta$, is also equal to zero. The "ideal" filter is created by the function:

$$F(S) = \frac{s + a}{S}$$

This second-order loop is most common; this requires the equivalent of two simple DPLL's on one chip for implementation of the most useful all-around product.

Third- and higher-order loops can also be implemented. However, due to the added complexity and loop stability problems, they find limited application and, hence, will not be discussed.

1. Analog PLL's

Analog PLL's are implemented with voltage-controlled oscillators; usually voltage control is effected via a varactor diode tuning a Colpitts-type oscillator. However, digital MV-type oscillators are also used with the disadvantage of nonlinear output waveforms. Phase detectors are usually simple exclusive OR gates or edge-sensitive (charge pump) digital detectors with out-of-lock detection logic. High-performance rf loops often use integrate-sample-and-hold phase detectors or balanced demodulators. Second-order analog PLL's use both passive and active filters; lead-lag filters usually provide the best tradeoffs between bandwidth, acquisition time, and loop stability.

Analog loops suffer the difficulties associated with analog signal processing techniques such as the inherent frequency drift of VCO's, i.e., jitter, natural solid-state noise, power supply disturbance, and temperature-related drift. Many PLL applications, requiring low fm deviation and low spurious levels (-50 to -100 dB), require tedious design and layout to keep analog VCO's sufficiently quiet. Likewise, analog amplifier and passive components, used in the second-order loop filter, produce natural noise and drift as well as temperature drift. Analog PLL's operating at low frequencies (under 100 Hz) are difficult to design for tight control due to VCO jitter, an area of significant advantage for digital PLL's.

2. Draper DPLL's

Figure A-3 shows a block diagram of the Draper Labs first-order DPLL. Here the phase (ϕ) detector can be a digital exclusive OR gate or edge-sensitive detector, same as for an analog loop. However, the difference lies in the use of a digital tracking filter for the VCO function. The Draper digital filter, described concisely in Refs. 1 and 2, is the up/down (U/P) counter and add/delete (increment/decrement) scheme.

Thus, VCO (digital filter) short- and long-term stability is as good as the clock (Mf_c), where f_c is the loop center frequency, and M is a multiple

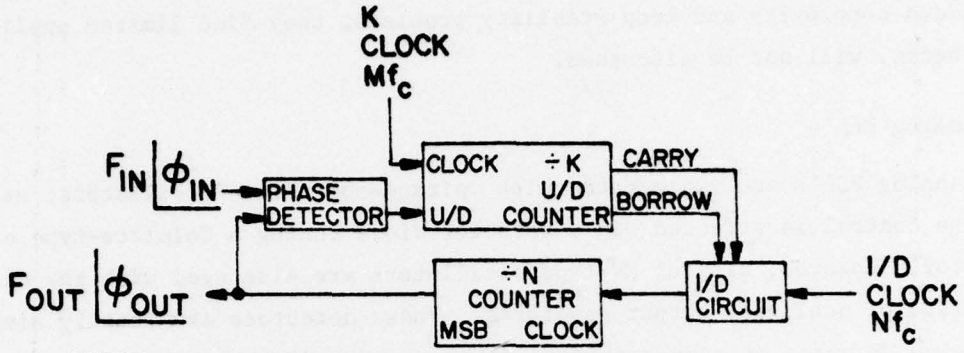

Figure A-3. First-order DPLL (Fig. 1 from Ref. 2).

of the center frequency based upon desired loop phase resolution. Length of the U/D counter depends upon loop bandwidths. Clearly, the frequency step error of the first-order DPLL depends upon the faster M. The instantaneous add/delete frequency increments (ϕ jumps) produce spurious sidebands in DPLL's that require attention in DPLL design. Since the digital filter frequency stability is dependent on the reference oscillator stability (highly accurate crystal-controlled oscillators may be used), a major DPLL application advantage, which will be illustrated later, lies in high-quality loop performance at low and ultralow center frequencies.

Another DPLL feature is the ability to digitally control the loop bandwidth by programming the K-counters shown in Fig. A-3. In analog loops, digital controls would change the loop bandwidth by switching RC components, an awkward and noise-prone - but feasible - design.

The digital filter also requires a ÷N counter to return the phase-corrected loop clock back to the loop center frequency. Implementation of the Draper DPLL, as described in Ref. 2, is achieved by the use of a CMOS LSI DPLL chip consisting of phase detector, K counter, and I/D (increment/decrement) counter in a 24-pin IC package. The variable ÷N function is a separate standard CMOS counter IC. The design has CMOS amplifier stages for implementing an RC or crystal-controlled clock.

Figure A-4 is a block diagram of a second-order DPLL which is analogous to the second-order analog PLL of Fig. A-2. Here two DPLL IC's and two ÷N counter IC's are used for a total of four chips. The references (1 and 2)

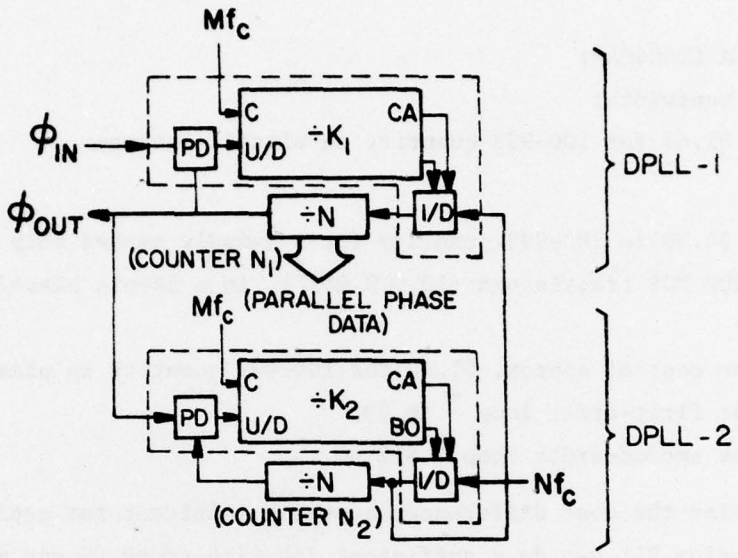

Figure A-4. Second-order DPLL (Fig. 9 from Ref. 1).

give examples of how the second-order loop can be augmented to extend the bandwidth and also provide digital rate data output, another feature of digital PLL's.

C. COMPARISON OF ANALOG PLL AND DRAPER DPLL IC's

1. Cost Comparisons

Historically the improvements in electronic system performance and economy have been achieved in most areas of information and signal processing by the conversion of analog circuit techniques to digital circuit techniques. This improved performance, initially at higher cost, ultimately results in equal or lower costs. Thus, at this time the promising DPLL performance improvements are at plus cost when Draper Labs DPLL IC costs are specifically compared to costs for similar-production-model analog PLL IC's. The approximate figures are shown below.

2. Analog PLL IC Examples

Bipolar PLL IC (Signetics 560B, 562B):

- 500-kHz bandwidth;
- approx. $2.50 for 100-999 quantity in plastic package.

CMOS PLL IC (RCA CD4046A):

- 500-kHz bandwidth;
- approx. $1.69 for 100-999 quantity in plastic package.

Draper DPLL IC:

- Approx. $4.90 in 100-999 quantity for a densely packed chip of about 1000 MOS transistors (10,000 mil^2), in a 24-pin plastic package;
- N-counter cost of approx. $1.40 for 100-999 quantity in plastic.
- Total for first-order loop $\approx$ $6.30.
- Total for second-order loop $\approx$ $12.60.

At this point the cost differences appear significant for applications in which the analog PLL can do a sufficient job with added RC and manufacturing trimming costs properly factored in. At present it is *important* to consider those DPLL applications where superior performance (to that of analog PLL's) is required, and where the DPLL performance is adequate to the job.

D. APPLICATIONS SURVEY

Areas of PLL IC applicability are limited primarily to operating frequency range. The low-cost general-purpose analog PLL's have an operating frequency of 0.5-1 MHz, with higher-cost ($6) IC's having a bandwidth out to 15 MHz. The Draper DPLL, implemented with the standard bulk CMOS process, has an upper limit for the clock input frequency of 5 MHz; with higher-speed CMOS processing at RCA, 15-20 MHz is now feasible. Depending on the application, we can generalize DPLL application for approx. 5-15 kHz ($\pm$0.1% phase resolution) in high-performance digital filtering and 50-150 kHz for loose frequency tracking needs, i.e., $\pm$10% phase resolution.

1. Demodulation

There are two major PLL use areas for fm demodulation: (1) digital data transmission (fsk) demodulation, and (2) low-threshold analog signal demodulation.

2. fsk Demodulation

For fsk demodulation of low-speed signals up to 600 baud, first-order DPLL's with clocks of 100-200 kHz are feasible. First-order loops having constant phase error are suitable, since second-order loops have peak phase errors that are disadvantageous to fsk demodulation. The use of a DPLL with high-speed SOS or C^2L* processing could make fsk demodulation of 50K-baud data channels practical; this application requires 10- to 20-MHz clocks for good performance. At the lower frequencies (100-600 baud) the DPLL is particularly attractive because it provides excellent frequency stability.

3. Low-Threshold Demodulation

At fm-radio i-f frequencies (10.7 MHz) the DPLL is too slow for demodulation purposes. At i-f frequencies below approx. 50 kHz, second-order DPLL's are feasible, but low-cost analog and non-PLL demodulation circuits are well entrenched; prospects for the use of the DPLL are therefore promising.

4. Frequency Synthesis

The use of PLL's in digital frequency synthesis has recently become increasingly important in commercial transceiving radio equipment for local-oscillator (LO) injection timing; military use has been widespread for the last five years. In these applications the spurious and harmonic content of the LO injection signal is required to be 50 to 100 dB below the carrier frequency. In most communications applications that involve LO frequency synthesis, the requirement for a high center frequency rules out the use of DPLL's because of the requirement for a clock rate of 1000 times the center frequency. (In order to keep digital quantizing noise or spurs 60 dB down from synthesizer LO signals, we can translate 60 dB into an equivalent phase resolution of 1/1000 of the VCO center frequency.) PLL's, on the other hand, have a relatively high center frequency.

*Closed CMOS Logic - RCA high-speed bulk CMOS layout and process.

Frequency synthesis by means of the second-order DPLL loop (Fig. A-4) would be attractive for applications of 5- to 15-kHz center frequency, making limited instrumentation applications feasible. Here the superior digital filter stability of the DPLL is important, say, for laboratory-quality audio-frequency synthesis. Stability during operation down to very low frequencies is another great advantage of a DPLL synthesizer; at low frequencies (less than $\tilde{\sim}$ 50 Hz) the analog VCO is too unstable.

5. Frequency Synchronization

Digital data modems and pocket-paging systems have a common need for frequency synchronization of an internal clock to the average data rate. Phase resolution of 5 to 30° is all that is necessary in many cases. The first-order loop is ideal for these applications, many of which require a center frequency of 1 to 5 kHz and a clock of 50 to 350 kHz.

A more stringent synchronization application involves a tracking navigation receiver; f_c is 1 to 15 kHz and phase resolution is approx. 1°. A 4- to 5-MHz clock makes this a practical application for a first-order DPLL. In these applications, input signals are often missing for long periods of time; hence the frequency stability of the DPLL VCO (digital filter) is advantageous in that, when the signal comes back, the VCO will not have drifted from its center frequency. Much use of the DPLL could be achieved in the frequency synchronization of digital modems *if* the cost of IC components were to come close to that of analog components. The DPLL technique may also be included as a portion of complete LSI address recognition chips (pocket pagers). Chips of this type are currently being used in conjunction with analog PLL circuits such as the 4046, with loose specification requirements on phase resolution. Frequency drift, however, *is* troublesome with analog PLL's in these cases.

6. Tone Recognition

In applications such as touch-tone decoding, remote control of TV, paging, and wireless intercom, tone-recognition PLL's are widely used. Tones ranging from 500 Hz to 2 kHz with a detection bandwidth of about 10% and an s/n ratio of 6 dB are usually required. Touch-tone decoders also need fast lock times: frequencies of 5 Hz or less. Second-order DPLL's with 200- to 500-kHz clocks

fit the application well, as do several analog IC PLL's now on the market; again, cost competitiveness would be a critical factor in bringing the DPLL to high-volume usage for tone recognition. Ideally the DPLL could be advantageous in digitally controlling the bandwidth for wide-band operation (fast pull-in) and then switching to narrow band for higher Q.

7. Frequency Multiplication

PLL's are commonly used to generate frequencies by locking onto the harmonics of signals which are rich in harmonics, such as square waves. In these applications narrow-band second-order PLL's are used. High Q's are requirements. References 1 and 3 give formulas for computing the length of the DPLL up/down counter that will set required Q's. The superior frequency stability of the DPLL is advantageous for this application.

8. Low-Frequency Phase-Angle Measurement

The DPLL appears to have optimum qualities for precise phase-angle discrimination in the presence of noise at low frequencies. One example of this application is the need of utility companies to measure average power factor for small phase angles. Average zero crossing of voltage and current with 10- to 40-ns jitter requires 5-μs phase resolution of 60 Hz. Average variations are tracked over a period of several seconds. A first-order DPLL with a 200-kHz clock is applicable; the added cost, compared to the cost of analog PLL's, is of minor importance here.

The DPPL is also useful in similar low-frequency, low-jitter filtering applications.

9. Motor-Control Applications

PLL's are used in various motor-control applications. Examples are 60-Hz motors, 30- to 40-kHz feedback control for a microfilm equipment (±10% phase accuracy), and 3-kHz tape recorder flutter measurement requiring 0.2-Hz resolution. A major manufacturer of magnetic tape recorders uses PLL's to control rotor speed. The f_c for the 54-r/s rotor is approx. 15 kHz; the DPLL clock would be 4-5 MHz for the required 1° of phase resolution at lock. The first-order DPLL fits more motor-control system control and measurement requirements. However, so do the low-cost general-purpose analog PLL IC's.

E. CONCLUSIONS AND RECOMMENDATIONS

DPLL's are available whose performance outdistances that of analog PLL's in many applications. Conclusions and recommendations of this study are as follows:

1. DPLL's offer outstanding frequency stability, surpassing any results obtainable with analog PLL's.
2. In many low-frequency PLL applications analog PLL's cannot be used at all or can be used only with great difficulty.
3. The need for high-speed clocking limits the use of DPLL's; the RCA high-speed SOS or C^2L process should be used for the DPLL.
4. The clock rate is critical in determining phase resolution and spurious components. The clocks actually generate added spurious components in the frequency output spectrum, and this limits the use of DPLL's in high-grade frequency synthesizers.
5. The DPPL is the ideal IC for low-frequency synchronization with a first-order loop (one loop, two IC's).
6. Higher cost will limit the use of DPLL's in the near future; single-chip second-order LSI designs are necessary to make possible the widespread use of DPLL's by 1978-80.

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3. S. Gupta, "Phase-Locked Loops," Proc. IEEE, 63, No. 2, Feb. 1975.